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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/640,349	08/12/2003	Yi-Fang Michael Shiuan	JCLA11051	7717

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4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	PAPER NUMBER
2629	
MAIL DATE	DELIVERY MODE
05/12/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/640,349	SHIUAN ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2010 and 04 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 17-20* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on *24 February 2010.* These drawings are acceptable.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. *Claim 18* is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Claim 18 recites, "***while executing the power saving process, the system memory is continuously accessed by the CPU during the non-responding period of the CPU***" (*lines 1-3*).

This subject matter is not described in the specification.

The Applicant alleges, "*In paragraph [0012] of the present invention,* ***'The present invention provides four different image data display mechanisms for continuously displaying image/graphics data on multiple display devices computer system that contains a system memory directly accessed by the computer's CPU during the non-responding period of the***

CPU.' *After the PSPP is executed, the CPU waits, and then falls into the non-responding period, and the system memory is* ***directly accessed*** *by the computer's CPU during the non-responding period of the CPU. Therefore, it has taught and disclosed that while executing the power saving process, the system memory is* ***continuously accessed*** *by the CPU during the non-responding period of the CPU*" (see page 11 of the *4 November 2009* Response). However, the examiner must respectfully disagree.

Although the instant Specification arguably provides a disclosure of "*a system memory directly accessed by the computer's CPU during the non-responding period of the CPU*"; the Specification nowhere teaches "*the system memory is continuously accessed by the CPU during the non-responding period of the CPU.*"

4. *Claim 18* is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 18 recites, "***while executing the power saving process, the system memory is continuously accessed by the CPU during the non-responding period of the CPU***" (*lines 1-3*).

This subject matter is not enabled by the specification.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. *Claims 1-4* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Shelton et al (US 6,046,709 A)*** in view of ***Koyama et al (US 2002/0021274 A1)***.

Regarding Claim 1, ***Shelton*** discloses a graphics display method for continuously displaying a plurality of graphics data [*e.g., a flight simulator program*] on multiple display devices [*e.g., Fig. 1; 113, 114, 116, 120*] of a computer system [*e.g., Fig. 1; 100, 102, 104*] (*e.g., see Column 6, Lines 11-27*),

the method comprising:

providing a common clock source [*e.g., Fig. 4; 420*] to the display devices and

synchronizing [*e.g., via frame and sync locking*] a plurality of blank periods [*e.g., vertical and horizontal blank periods*] of the display devices according to the common clock source; and

executing a power saving process [*e.g. not refreshing every display device as fast as possible*] within a least common multiple occurrence of the blank periods of the display devices [*e.g., due to the slowest graphics board*] (*see the entire document, including Column 4, Line 18 - Column 8, Line 20*).

Shelton teaches, "*the master graphics board preferably also has* ***a reference clock generator 420*** *that is* ***used to drive all reference clock lines for all synchronization cards and graphics boards*** *within the system.* ***This clock signal forms the basis for synchronizing video timing and buffer swaps***" (see Column 15, Lines 17-24).

Shelton continues, "***The vertical blank period should occur almost simultaneously for all monitors, due to sync locking, resulting in all displays 113, 114, 116 almost simultaneously switching to the next frame in a corresponding set of frames. Such coordination is achieved by synchronizing the graphics boards 120 through an initialization process that sets all boards to the same horizontal and vertical refresh frequencies, and directs the boards to follow a common clock signal for timing initiation of the vertical refresh. This initialization is partially controlled by the frame synchronization card***" (see Column 7, Line 53 - Column 8, Line 5).

As such, Shelton clearly discloses using a common clock source to synchronize blank periods of the display devices, as instantly claimed.

Shelton does not appear to disclose the *particular computer (CPU + GPU) circuitry arrangement*, as instantly claimed.

However, ***Koyama*** discloses a graphics display method for continuously displaying a plurality of graphics data [*e.g., image data*] on a display device [*e.g., Fig. 24; pixel portion*] of a computer system [*e.g., Fig. 24*] that contains

a central processing unit [*e.g., Fig. 24; CPU 2408*] which has a memory controller [*e.g., Fig. 24; 2407*] inside the CPU,

a graphics-processing unit [*e.g., Fig. 24; 2412*] coupled to the memory controller, and

a system memory [*e.g., Fig. 24; 2411*] directly accessed by the CPU,

wherein the display device is coupled [*e.g., Fig. 24; via 2413*] to the graphics-processing unit,

the method comprising:

providing a common clock source [*e.g., Fig. 24: start pulses, clock signals provided by 2412*] to the display device and

synchronizing a plurality of blank periods [*e.g., via row and column driving periods*] of the display devices according to the common clock source (*e.g., see Paragraph 120*);

receiving a power saving signal from the CPU [*e.g., still image mode judgment signal*],

the power saving signal indicates a request for executing a power saving process [*e.g., still image mode*] by the CPU during a non-responding period of the CPU [*e.g., period when a still image is displayed until a changed image is input from external interface port 2405*],

so as to reduce consumptive power of the CPU [*e.g., via selective stopping certain CPU operations*],

wherein memory access from the graphics-processing unit to the system memory through memory controller is blocked [*e.g., by stopping reading operations of data from VRAM 2411*] during the non-responding period of the CPU; and

executing the power saving process within an occurrence of the blank periods [*e.g., wherein still images are capable of lasting for multiple consecutive frames, so as to include many vertical and horizontal blanking periods*] of the display device (*see the entire document, including Paragraphs 118-125*).

Shelton and ***Koyama*** are analogous art, because they are from the shared inventive field of computer systems having displays that operate to reduce power consumption.

Therefore, it would have been obvious to use ***Koyama's*** computer [*e.g., Fig. 24, Paragraph 2*] to form at least one of ***Shelton's*** networked computers [*e.g., Fig. 1: 100, 102, 104*], so as to reduce power consumption while still images are displayed.

Regarding Claim 2, ***Shelton*** discloses a step of detecting an upcoming least common multiple occurrence of the blank periods of the display devices before [*e.g., while displaying changing/motion images*] the executing the power saving process (*e.g., see Column 4, Line 47 - Column 5, Line 15; Column 10, Lines 20-43*).

Regarding Claim 3, ***Shelton*** discloses the blank periods can be a plurality of horizontal blank periods (*e.g., see Column 4, Line 47 - Column 5, Line 15*).

Regarding Claim 4, ***Shelton*** discloses the horizontal blank periods are provided by a graphics-processing unit [*Fig. 2; 208, 210, 218, 220*] (*e.g., see Column 8, Lines 6-20*).

Koyama also discloses the horizontal blank periods are provided [*e.g., Fig. 24: to the driving circuits*] by the graphics-processing unit (*e.g., see Paragraphs 119-120*)

8. *Claim 17* is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Shelton et al (US 6,046,709 A)*** in view of ***Koyama et al (US 2002/0021274 A1)*** and ***White et al (US 7,634,668 B2)***.

Regarding Claim 17, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, ***Koyama*** discloses the power saving signal indicates a request for executing a power saving process to make the CPU self-adjust a power level [*e.g., via selectively stopping unnecessary CPU operations*] of the CPU (*e.g., see Paragraphs 118-125*).

Neither ***Shelton*** nor ***Koyama*** appears to expressly disclose *adjusting the CPU-clock rate*, as instantly claimed.

However, ***White*** discloses a graphics display method comprising: executing a power saving process to make a CPU [*e.g., Fig. 1: 102*] self-adjust a CPU-clock rate [*e.g., Fig. 1: via 114*] and a power level of the CPU (*see the entire document, including Figs. 5-6; Column 3, Line 15 - Column 7, Line 20*).

Shelton, ***Koyama***, and ***White*** are analogous art, because they are from the shared inventive field of computer systems for controlling displays that operate to reduce power consumption.

Therefore, it would have been obvious to use ***White's*** power saving techniques with ***Koyama's*** CPU [*e.g., Fig. 24: 2406*], so as to further reduce CPU power consumption.

9. *Claim 18* is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Shelton et al (US 6,046,709 A)***, ***Koyama et al (US 2002/0021274 A1)***, and ***White et al (US 7,634,668 B2)*** as applied to *claim 17* above, and further in view of ***Sheaffer et al (US 6,593,930 B1)***.

Regarding Claim 18, ***Koyama*** discloses while executing the power saving process, the system memory is continuously accessed by the CPU during the non-responding period of the CPU (*e.g., see Paragraph 49 -- wherein reading VRAM data is stopped, but not writing data*).

Should it be shown that ***Koyama*** discloses *continuous memory access*, as instantly claimed, with insufficient specificity:

Sheaffer discloses while executing a power saving process [*e.g., memory shutdown period*], a system memory [*e.g., Fig. 1A: 104*] is continuously accessed by a CPU [*e.g., Fig. 1A: 100*] (*see the entire document, including Column 2, Line 43 - Column 5, Line 50*).

Shelton, ***Koyama***, ***White***, and ***Sheaffer*** are analogous art, because they are from the shared inventive field of computer systems having displays and memory that operate to reduce power consumption.

Therefore, it would have been obvious to use ***Sheaffer's*** memory maintenance techniques with ***Koyama's*** memory [*e.g., Fig. 24: 2411*], so as to prevent performance degradation and memory loss.

Response to Arguments

10. Applicant's arguments filed on *4 November 2009* have been fully considered but they are not persuasive.

The Applicant alleges, "*In paragraph [0012] of the present invention, '**The present invention provides four different image data display mechanisms for continuously displaying image/graphics data on multiple display devices computer system that contains a system memory directly accessed by the computer's CPU during the non-responding period of the CPU.**' After the PSPP is executed, the CPU waits, and then falls into the non-responding period, and the system memory is **directly accessed** by the computer's CPU during the non-responding period of the CPU. Therefore, it has taught and disclosed that while executing the power saving process, the system memory is **continuously accessed** by the CPU during the non-responding period of the CPU*" (see page 11 of the *4 November 2009* Response). However, the examiner must respectfully disagree.

Although the instant Specification arguably provides a disclosure of "*a system memory directly accessed by the computer's CPU during the non-responding period of the CPU*"; the Specification nowhere teaches "*the system memory is continuously accessed by the CPU during the non-responding period of the CPU*," as instantly claimed.

Applicant's arguments with respect to *claims 1-4, 17, and 18* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
5 May 2010